MODEL: TT4761B01-4

Ver. 1.1

Date: 31.May.2013

Customer's Approval	CSOT
Signature Date	Approved By Product Director Date Name: Richard Lung Signature:
	Reviewed By PM Manager Date Name: Aaron Tu Signature:
	Reviewed By Project Leader Date Name: KC Lee Signature:
	Reviewed By PM Date Name: Zou Yingnan Signature:

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Revision History

Version	Date	Page (New)	Section	Description	Revision by
Ver. 0.1	08.May.2013	24	9	Tentative Specification was First Issued.	Zou Yingnan
Ver. 1.1	31.May.2013	34	9	Preliminary Specification was First Issued	Zou Yingnan

1. General Description

1.1 Product Features

- **FHD Resolution (1920 x 1080)**
- **Very High Contrast Ratio:4000:1**
- **Fast Response Time**
- **Ultra Wide Viewing Angle: 178° (H)/178° (V)(CR≥10)**
- **DE (Data Enable) Mode**
- **LVDS (Low Voltage Differential Signaling) Interface**

1.2 Overview

TT4761B01-4,2D model, is a model name for CSOT internal use only. It includes the following components: Open Cell, Control Board and FFC.

TT4761B01-4 Components	
Open cell Model Name	ST4761B01-3
Control Board part no.	34291100006031
FFC part no.	39TL1000000005

ST4761B01-4 is a diagonal 47.6”color active matrix LCD open cell with 2ch-LVDS interface. This open cell is a transmissive type display operating in the normally black mode. It supports 1920x1080 FHD resolutions and can display up to16.7M colors (8bit). Each pixel is divided into Red, Green and Blue sub-pixels which are arranged in vertical stripe.

This open cell dedicates for LCD TV products and provides excellent performance which includes high transparency, ultra wide viewing angle and high color depth. CSOT open cell comply with RoHS for identification.

1.3 General Information

Item	Specification	Unit	Note
Active Area	1054.08(H)x592.92(V)	mm	
Cell Size	1068.750(H) x 607.610 (V) x 1.350 (D)	mm	
Weight	2.0	kg	Max.
Driving Scheme	a-Si TFT Active Matrix	-	
Pixel Pitch (Sub Pixel)	0.183 (H) x 0.549 (V)	mm	
Pixel Arrangement	RGB Vertical Stripe	-	
Display Colors	16.7 M	color	8bit
Display Mode	Transmissive Mode, Normally Black	-	
Glass Thickness (Array/CF)	0.5/0.5	mm	
Color Chromaticity	R=(0.639,0.335) G=(0.319,0.626) B=(0.155,0.052) W=(0.280,0.290)		Typical value measured at CSOT’s module: MT4761B01-1
Cell Transmittance	5.6 (Typ.)	%	
Polarizer(CF side)	Anti-glare, Haze2%, Hard Coating(3H)		
Polarizer(TFT side)	Hard Coating(3H)		

2. Absolute Maximum Ratings

2.1 Absolute Maximum Ratings (T_A= 25 ± 2 °C)

The followings are maximum values which, if exceeded, may cause damage to the unit.

Item	Symbol	Value		Unit
		Min.	Max.	
Power Supply Voltage	V_{CC}	-0.3	13.8	V
Input Signal Voltage	V_{IN}	-0.3	4.0	V

2.2 Environment Requirement (Based on CSOT Module MT4761B01-1)

(1) Temperature and relative humidity range are shown as below.

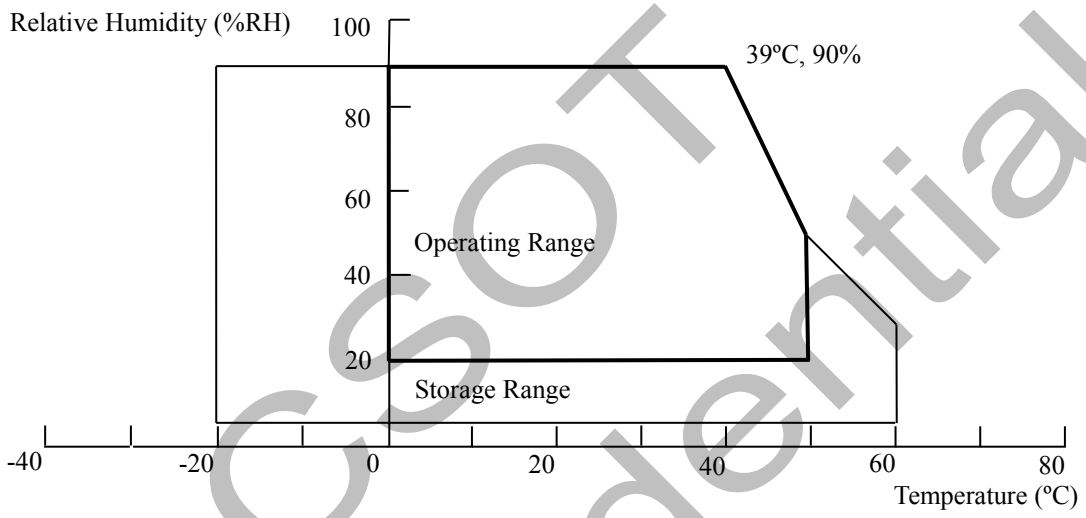


Fig. 2.1Operating and storage environment

(a) 90%RH maximum (T_A≤39 ºC).

(b) Wet-bulb temperature should be 39ºCmaximum (T_A>39 ºC).

(c) No condensation.

(2) The storage temperature is between - 20 ºC to 60 ºC, and the operating ambient temperature is between 0 ºC to 50 ºC. The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65ºC with LCD module in a temperature controlled chamber alone. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65ºC. The range of operating temperature may degrade in case of improper thermal management in the end product design.

(3) The rating of environment is based on LCD module. Leave LCD cell alone, this environment condition can't be guaranteed. Except LCD cell, the customer has to consider the ability of other parts of LCD module and LCD module process.

2.3 Absolute Ratings of Environment (Open Cell)

When storing open cell as spares for a long time, please follow the precaution instructions:

(1) Do not store the module in high temperature and high humidity for a long time. It is highly recommended to store the module with temperature from20ºC to 30ºCin normal humidity (50±10%RH) with shipping package.

(2) The open cell should be keep within one month shelf life

3. Electrical Specification

3.1 Open Cell Power Consumption (TA = 25 ± 2 °C)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12.0	13.2	V	(1)
Rush Current		I_{RUSH}	-	-	2.0	A	(2)
Power Supply Current	White Pattern	I_{CC}	-	0.27	0.35	A	(3)
	Horizontal Stripe	I_{CC}	-	0.56	0.73	A	
	Black Pattern	I_{CC}	-	0.26	0.34	A	

Note:

(1)The ripple voltage should be controlled less than10% of V_{CC}.

(2)Measurement condition: $V_{CC=12V,}$ rising time=470μs.

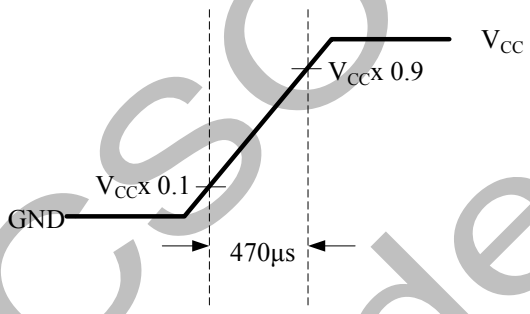
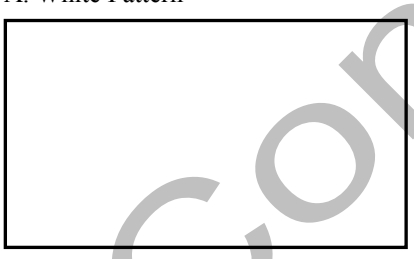


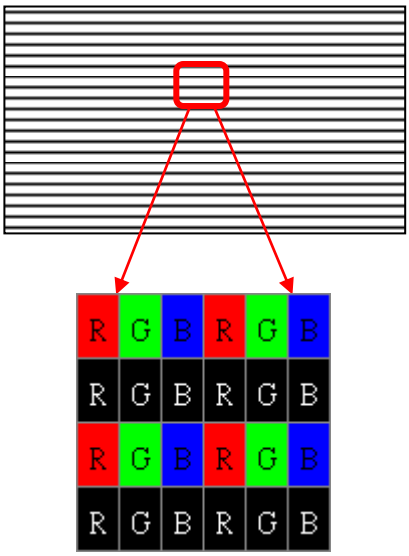
Fig. 3.1 V_{CC} rising time condition

(3)Measurement condition: V_{CC}=12V, Ta = 25 ± 2ºC, F = 60 Hz. The test patterns are shown as below.

A. White Pattern



B. Horizontal Pattern



C. Black Pattern

Fig. 3.2 Test patterns

3.2 LVDS Characteristics

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
LVDS Interface	Differential Input High Threshold Voltage	V_{TH}	+100	-	-	mV	(1)
	Differential Input Low Threshold Voltage	V_{TL}	-	-	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential Input Voltage	$\|V_{ID}\|$	200	400	600	mV	
	Terminating Resistor	R_T	87.5	100	112.5	ohm	
CMOS Interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note:

(1) The LVDS input signal has been defined as follows:

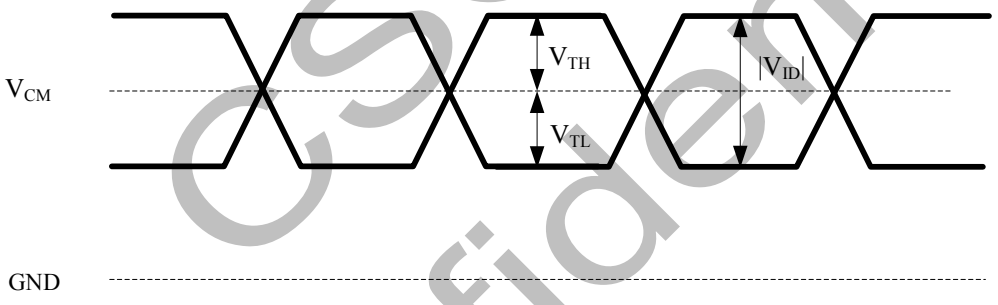


Fig. 3.3 LVDS input signal

4. Input Terminal Pin Assignment

4.1 Interface Pin Assignment

CN1: 187147-51221-3 (P-TWO) or equivalent (see Note (1))

Pin No.	Symbol	Description	Note
1	12V	DC power supply	
2	12V	DC power supply	
3	12V	DC power supply	
4	12V	DC power supply	
5	12V	DC power supply	
6	NC	No Connection	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	RO[0]N	Odd LVDS Signal -	
11	RO[0]P	Odd LVDS Signal +	
12	RO[1]N	Odd LVDS Signal -	
13	RO[1]P	Odd LVDS Signal +	
14	RO[2]N	Odd LVDS Signal -	
15	RO[2]P	Odd LVDS Signal +	
16	GND	Ground	
17	ROCLK-	Odd LVDS Clock -	
18	ROCLK+	Odd LVDS Clock +	
19	GND	Ground	
20	RO[3]N	Odd LVDS Signal -	
21	RO[3]P	Odd LVDS Signal +	
22	NC	No Connection	
23	NC	No Connection	
24	GND	Ground	
25	RE[0]N	Even LVDS Signal -	
26	RE[0]P	Even LVDS Signal +	
27	RE[1]N	Even LVDS Signal -	
28	RE[1]P	Even LVDS Signal +	
29	RE[2]N	Even LVDS Signal -	
30	RE[2]P	Even LVDS Signal +	
31	GND	Ground	
32	ROCLK-	Even LVDS Clock -	
33	ROCLK+	Even LVDS Clock +	

34	GND	Ground	
35	RE[3]N	Even LVDS Signal -	
36	RE[3]P	Even LVDS Signal +	
37	NC	No Connection	
38	NC	No Connection	
39	GND	Ground	
40	NC	No Connection	
41	NC	No Connection	
42	NC	No Connection	
43	NC	No Connection	
44	NC	No Connection	
45	LVDS_SEL	LVDS Data Format Selection	(2)
46	NC	No Connection	(3)
47	NC	No Connection	(3)
48	NC	No Connection	(3)
49	SCL	I2C Serial Clock (for adjust VCOM)	
50	SDA	I2C Serial Data (for adjust VCOM)	
51	WP	Write Protect (High: Write Enable, Low or Open: Write Disable)	

Note:

(1) The direction of pin assignment is shown as below:

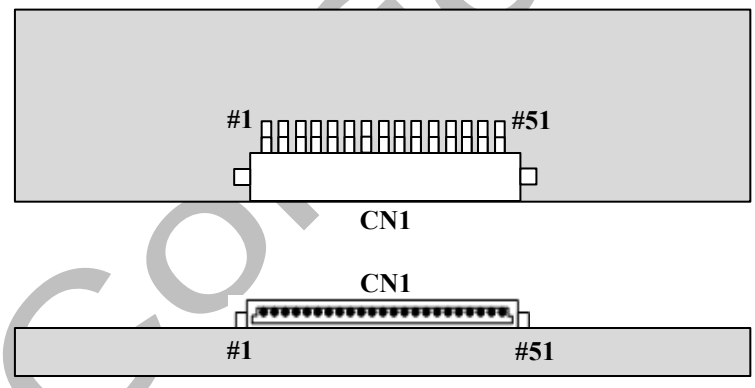
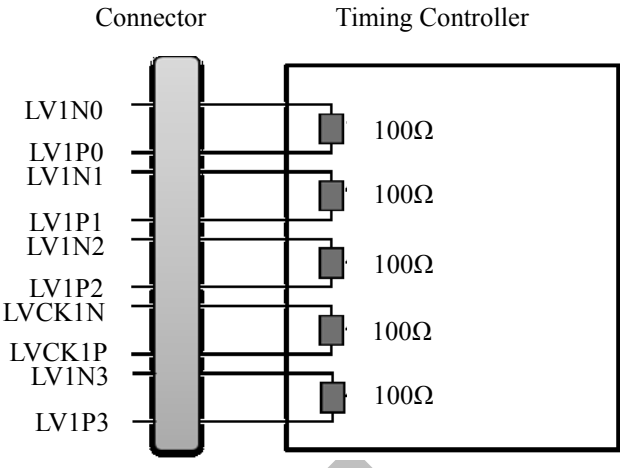


Fig. 4.1 LVDS connector direction sketch map

(2) High: connect to + 3.3 V → VESA format; Low: connect to GND or Open → JEIDA format.

(3) For CSOT internal only, please let it open.

4.2 Block Diagram of Interface



Attention:

(1) This open cell uses a 100 ohms (Ω) resistor between positive and negative lines of each receiver input.

(2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line respectively.

4.3 LVDS Interface

4.3.1 VESA Format (SELLVDS = H)

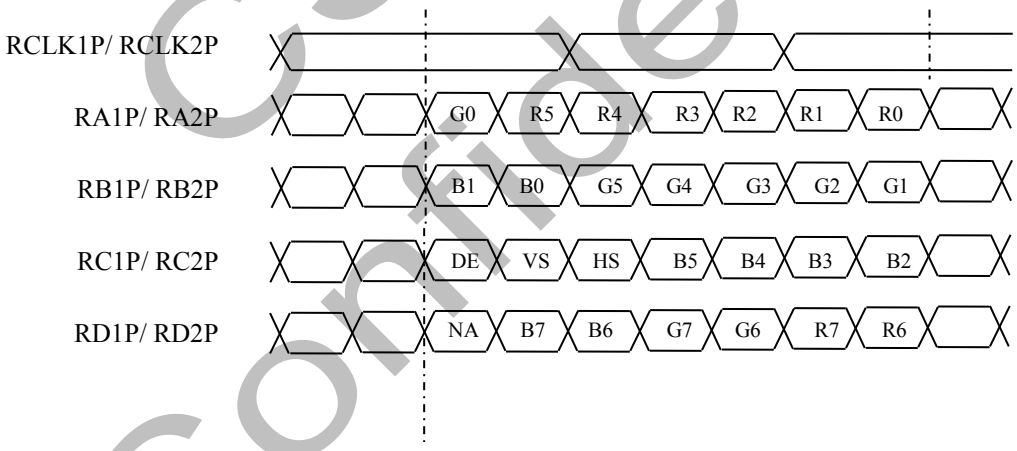


Fig. 4.2 VESA format

4.3.2 JEIDA Format (SELLVDS = L or Open)

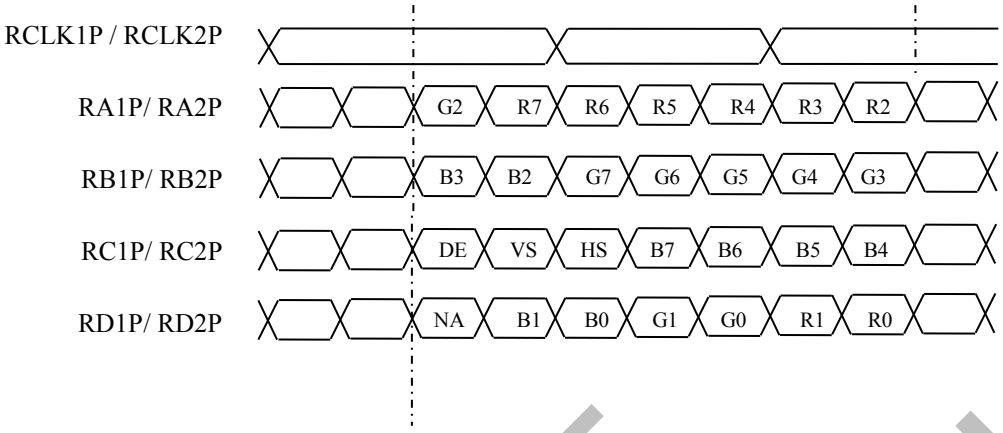
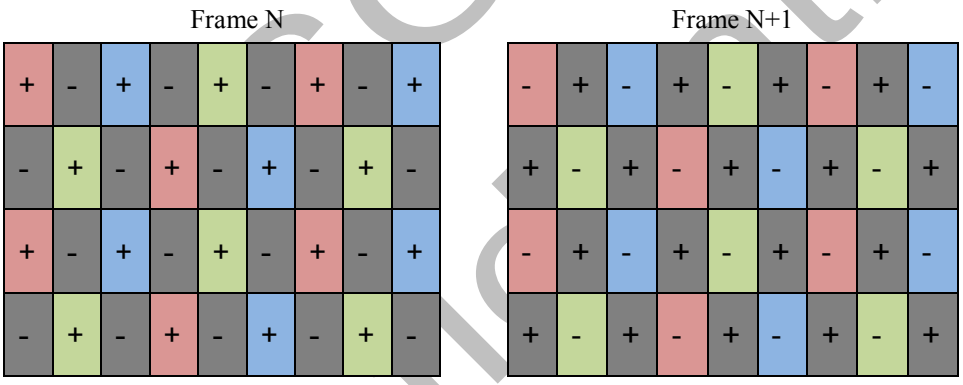


Fig. 4.3 JEIDA format

4.4 Pattern FOR Vcom Adjustment

Dot - inversion pattern



5. Interface Timing and Power On/Off Sequence

5.1 Timing Table (DE Only Mode)

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	Fclkin (=1/T_{Clk})	65	74.25	80	MHz	(1)
	Input cycle to cycle jitter	Trcl	—	—	200	ps	(2)
	Spread spectrum modulation range	Fclkin_mod	Fclkin-2%	—	Fclkin+2%	MHz	(3)
	Spread spectrum modulation frequency	F_{SSM}	—	—	200	KHz	
LVDS Receiver Data	Receiver Skew Margin	T_{RSM}	-400	—	400	ps	(4)
Vertical Active Display Term	Frame Rate	F	48	60	62.5	Hz	
	Total	T_V	1092	1125	1380	T_H	$T_V = T_{VD}$ +TVB
	Display	T_{VD}	1080			T_H	
	Blank	T_{VB}	12	45	300	T_H	
Horizontal Active Display Term	Total	T_H	1046	1100	1174	T_{CLK}	$T_H = T_{HD} + T_{HB}$
	Display	T_{HD}	960			T_{CLK}	
	Blank	T_{HB}	86	140	214	T_{CLK}	

Notes:

(1) Please make sure the range of pixel clock follows the following equations:

$T_{CLK}in(max) \geq Fmax \times T_V \times T_H$ $Fmin \times T_V \times T_H \geq T_{CLK}in(min)$

T_V

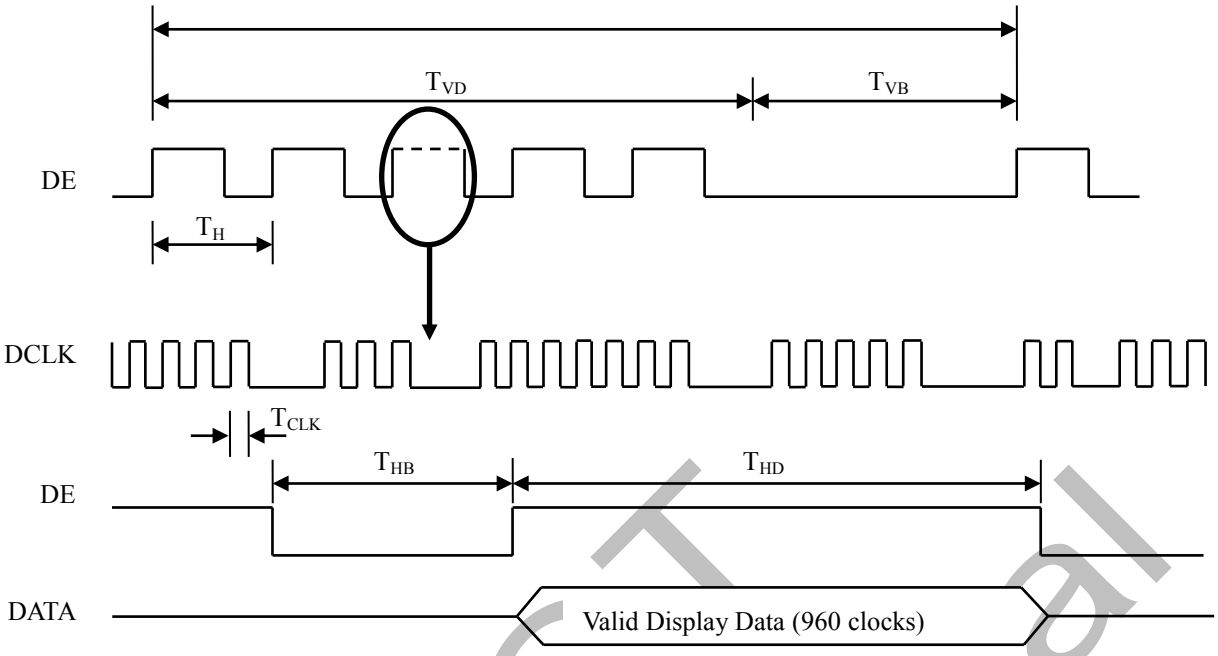


Fig. 5.1 Interface signal timing diagram

(2)The input clock cycle-to-cycle is defined as below figures.

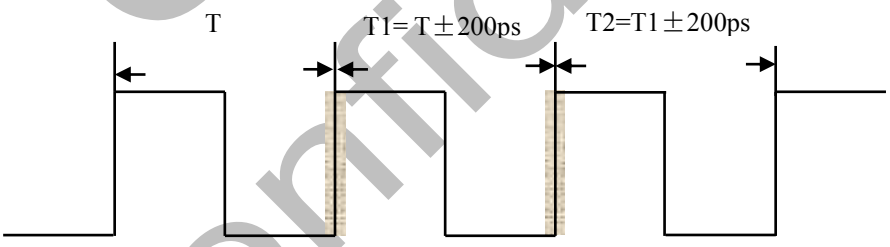


Fig. 5.2 Jitter

(3) The SSCG (Spread Spectrum Clock Generator) is defined as the following figure.

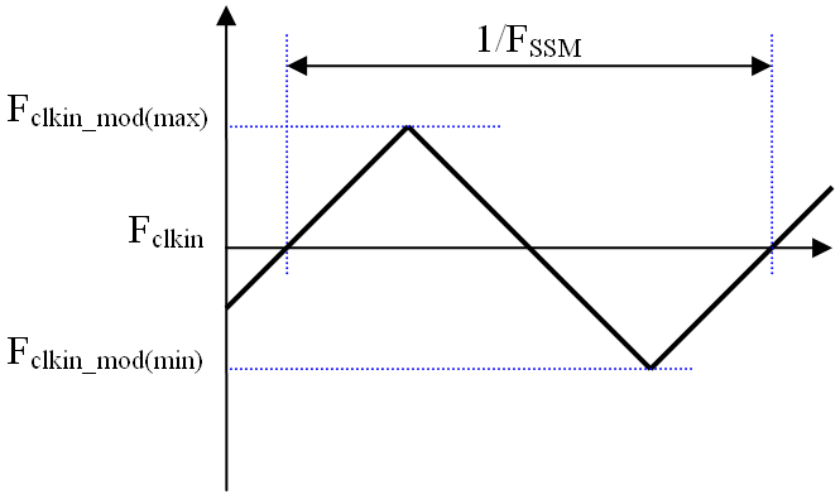


Fig.5.3 Spread Spectrum Clock diagram

(4) The LVDS timing diagram and setup/hold time is defined and showed as the following figure.

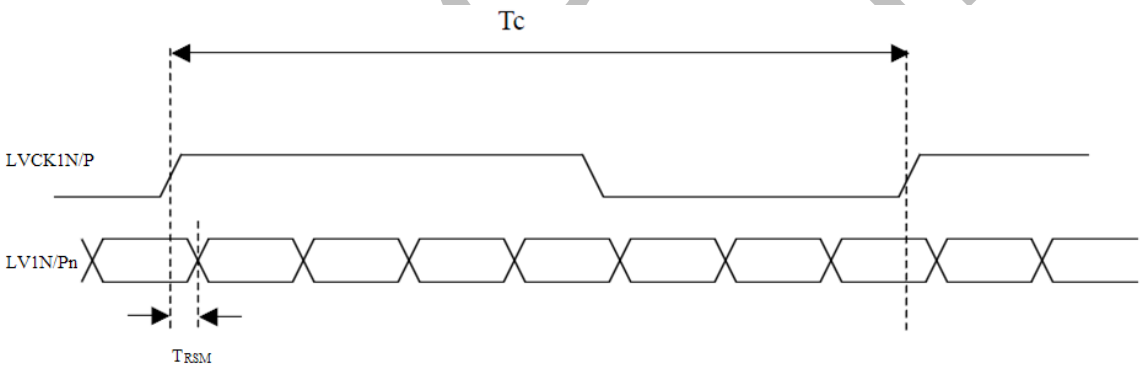


Fig.5.4 LVDS receive interface timing diagram

5.2 Power On/Off Sequence

To prevent a latch-up or DC operation of the Open cell, the power on/off sequence should be as the diagram below.

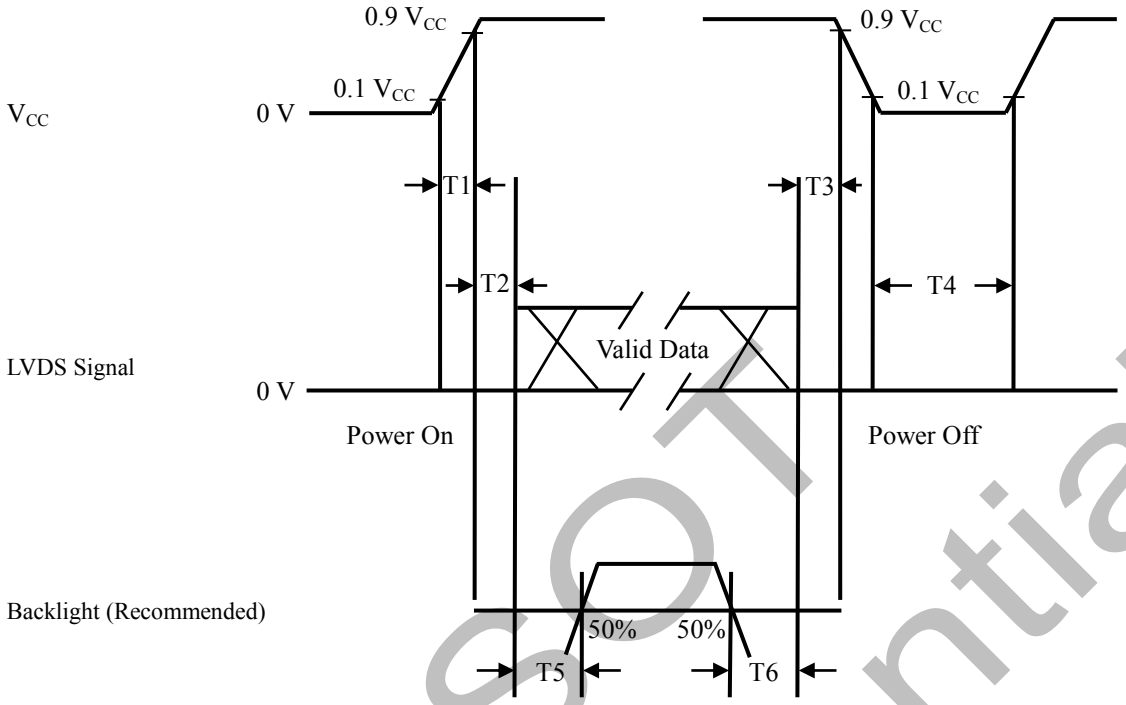


Fig. 5.2 Power On/Off

Parameter	Values			Unit
	Min.	Typ.	Max.	
T1	0.5	-	10	ms
T2	0	-	50	ms
T3	0	-	50	ms
T4	1000	-	-	ms
T5	500	-	-	ms
T6	100	-	-	ms

Attention:

(1) The supply voltage of the external system for the open cell input should follow the definition of VCC.

(2) When the customer's backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

(3) In case that VCC is in off level, please keep the level of input signals on the low or high impedance. If T2 < 0, that may cause electrical overstress.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

6. Optical Characteristics

6.1 Measurement Conditions

The table below is the test condition of optical measurement.

Item	Symbol	Value	Unit
Ambient Temperature	T_A	25±2	ºC
Ambient Humidity	H_A	50±10	%RH
Supply Voltage	V_{CC}	12	V
Driving Signal	Refer to the typical value in Chapter 3: Electrical Specification		
Vertical Refresh Rate	F_R	60	Hz

To avoid abrupt temperature change during optical measurement, it's suggested to warm up the LCD module more than 60 minutes after lighting the backlight and in the windless environment.

To measure the LCD cell, it is suggested to set up the standard measurement system as Fig. 6.1. The measuring area S should contain at least 500 pixels of the LCD cell as illustrated in Fig.6.2(A means the area allocated to one pixel).In this model, for example, the minimum measuring distance Z is 370mm when θ is 2 degree. Hence, 500mm is the typical measuring distance. This measuring condition is referred to 301-2H of VESA FPDM 2.0 about viewing distance, angle, and angular field of view definition.

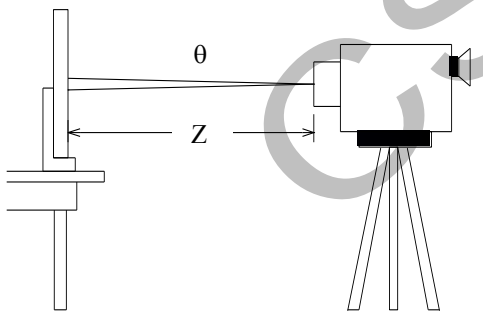


Fig. 6.1The standard set-up system of measurement

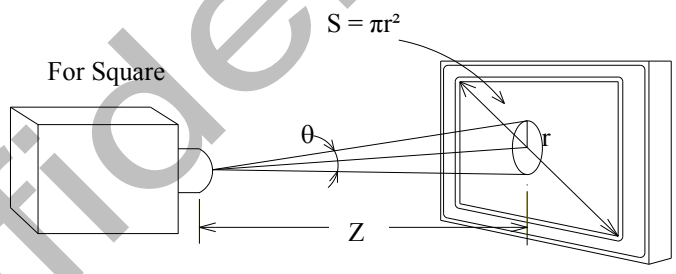


Fig. 6.2The area S contains at least 500 pixels to be measured

$$N = \frac{S}{A} \geqslant 500\text{pixels}$$

N means the actual number of the pixels in the area S.

6.2 Optical Specifications

The table below of optical characteristics is measured by MINOLTA CS2000, MINOLTA CA310, ELDIM OPTI Scope-SA and ELDIM EZ Contrast in dark room.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Static Contrast Ratio		CR	θ_H=0°, θ_V=0° Normal direction at center point with CSOT's module: MT4761B01-1	-	4000	-	-	(1) (2)
Response Time		T_L		-	6.5	12	ms	(3)
Center Transmittance		T%		-	5.6		%	(2)(4)
Color Chromaticity (CIE1931)	Red	R_X		Typ. - 0.03	0.633	Typ. +0.03	-	(2) (5)
		R_Y			0.334		-	
	Green	G_X			0.322		-	
		G_Y			0.631		-	
	Blue	B_X			0.159		-	
		B_Y			0.049		-	
	White	W_X			0.280		-	
		W_Y			0.290		-	
	Color Gamut	CG		-	72	-	% NTSC	
Viewing Angle	Horizontal	θ_{H+}	CR≥10	-	89	-	Deg.	(6)
		θ_{H-}		-	89	-		
	Vertical	θ_{V+}		-	89	-		
		θ_{V-}		-	89	-		

Note:

(1)Definition of static contrast ratio (CR):

It's necessary to switch off all the dynamic and dimming function when measuring the static contrast ratio.

$$\text{Static Contrast Ratio (CR)} = \frac{\text{CR-W}}{\text{CR-D}}$$

CR-W is the luminance measured by LMD (light-measuring device) at the center point of the LCD module with full-screen displaying white. The standard setup of measurement is illustrated in Fig. 6.3; CR-D is the luminance measured by LMD at the center point of the LCD module with full-screen displaying black. The LMD in this item is CS2000.

(2)The LMD in the item could be a spectroradiometer such as (KONICA MINOLTA) CS2000, CS1000 (TOPCON), SR-UL2 or the same level spectroradiometer. Other display color analyzer (KONICA MINOLTA) CA210, CA310 or (TOPCON) BM-7 could be involved after being calibrated with a spectroradiometer on each stage of a product.

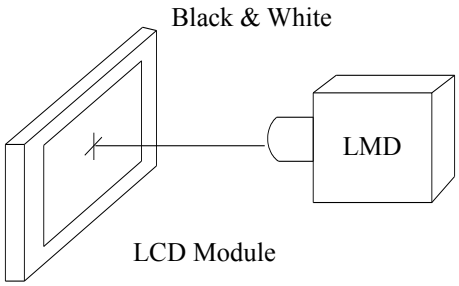


Fig. 6.3 The standard setup of CR measurement

(3) Response time T_L is defined as the average transition time in the response time matrix. The table below is the response time matrix in which each element $t_{X\ to\ Y}$ is the transition time from luminance ratio X to Y. X and Yare two different luminance ratiosamong0%,25%,50%,75%, and 100%luminance. The transition time $t_{X\ to\ Y}$ is defined as the time taken from 10% to 90% of the luminance difference between X and Y (X<Y) as illustrated in Fig.6.4. When X>Y, the definition of $t_{X\ to\ Y}$ is the time taken from 90% to 10% of the luminance difference between X and Y. The response time is optimized on refresh rate F_r=60Hz.

Measured Transition Time		Luminance Ratio of Previous Frame				
		0%	25%	50%	75%	100%
Luminance Ratio of Current Frame	0%		$t_{25\%\ to\ 0\%}$	$t_{50\%\ to\ 0\%}$	$t_{75\%\ to\ 0\%}$	$t_{100\%\ to\ 0\%}$
	25%	$t_{0\%\ to\ 25\%}$		$t_{50\%\ to\ 25\%}$	$t_{75\%\ to\ 25\%}$	$t_{100\%\ to\ 25\%}$
	50%	$t_{0\%\ to\ 50\%}$	$t_{25\%\ to\ 50\%}$		$t_{75\%\ to\ 50\%}$	$t_{100\%\ to\ 50\%}$
	75%	$t_{0\%\ to\ 75\%}$	$t_{25\%\ to\ 75\%}$	$t_{50\%\ to\ 75\%}$		$t_{100\%\ to\ 75\%}$
	100%	$t_{0\%\ to\ 100\%}$	$t_{25\%\ to\ 100\%}$	$t_{50\%\ to\ 100\%}$	$t_{75\%\ to\ 100\%}$	

$t_{X\ to\ Y}$ means the transition time from luminance ratio X to Y.

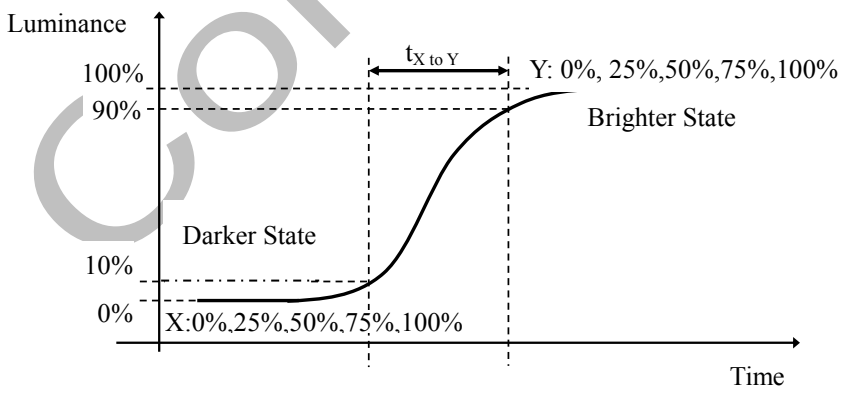


Fig. 6.4 The definition of $t_{X\ to\ Y}$

All the transition time is measured at the center point of the LCD module by ELDIM OPTI Scope-SA.

(4) Definition of center Transmittance (T%):

The transmittance is measured with full white pattern (Gray 255)

$$\text{Static Contrast Ratio (CR)} = \frac{\text{Luminance of LCD module}}{\text{Luminance of Backlight}}$$

(5) Definition of color chromaticity:

Each chromaticity coordinates (x, y) are measured in CIE1931 color space when full-screen displaying primary color R, G, B and white. The color gamut is defined as the fraction in percent of the area of the triangle bounded by R, G, B coordinates and the area is defined by NTSC 1953 color standard in the CIE color space. Chromaticity coordinates are measured by CS2000 and the standard setup of measurement is shown in Fig. 6.5.

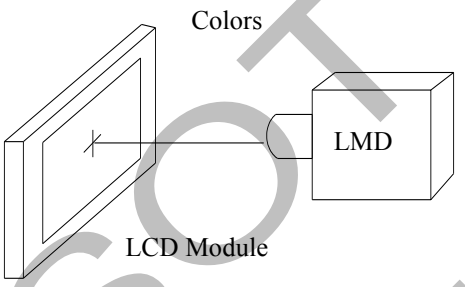


Fig. 6.5 The standard setup of color chromaticity measurement

(6)Definition of viewing angle coordinate system (θ_H,θ_V):

The contrast ratio is measured at the center point of the LCD module. The viewing angles are defined at the angle that the contrast ratio is larger than 10 at four directions relative to the perpendicular direction of the LCD module(two vertical angles: up θ_{V+} and downθ_{V-}; and two horizontal angles: right θ_{H+} and leftθ_{H-}) as illustrated in Fig. 6.6. The contrast ratio is measured by ELDIM EZ Contrast.

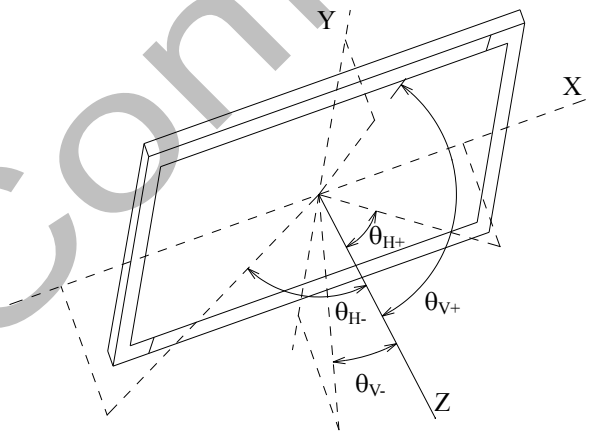
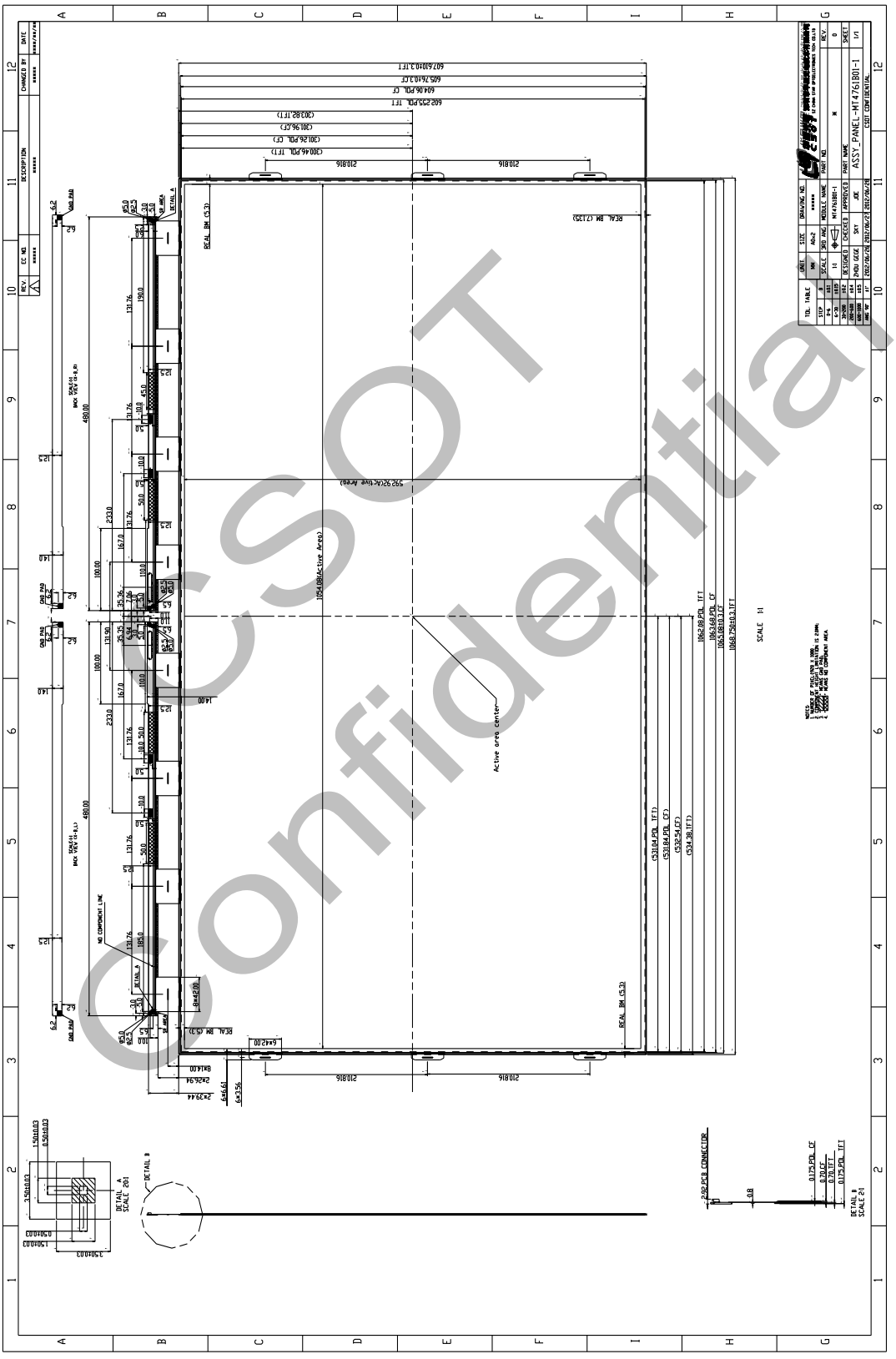


Fig. 6.6 Viewing angle coordination system

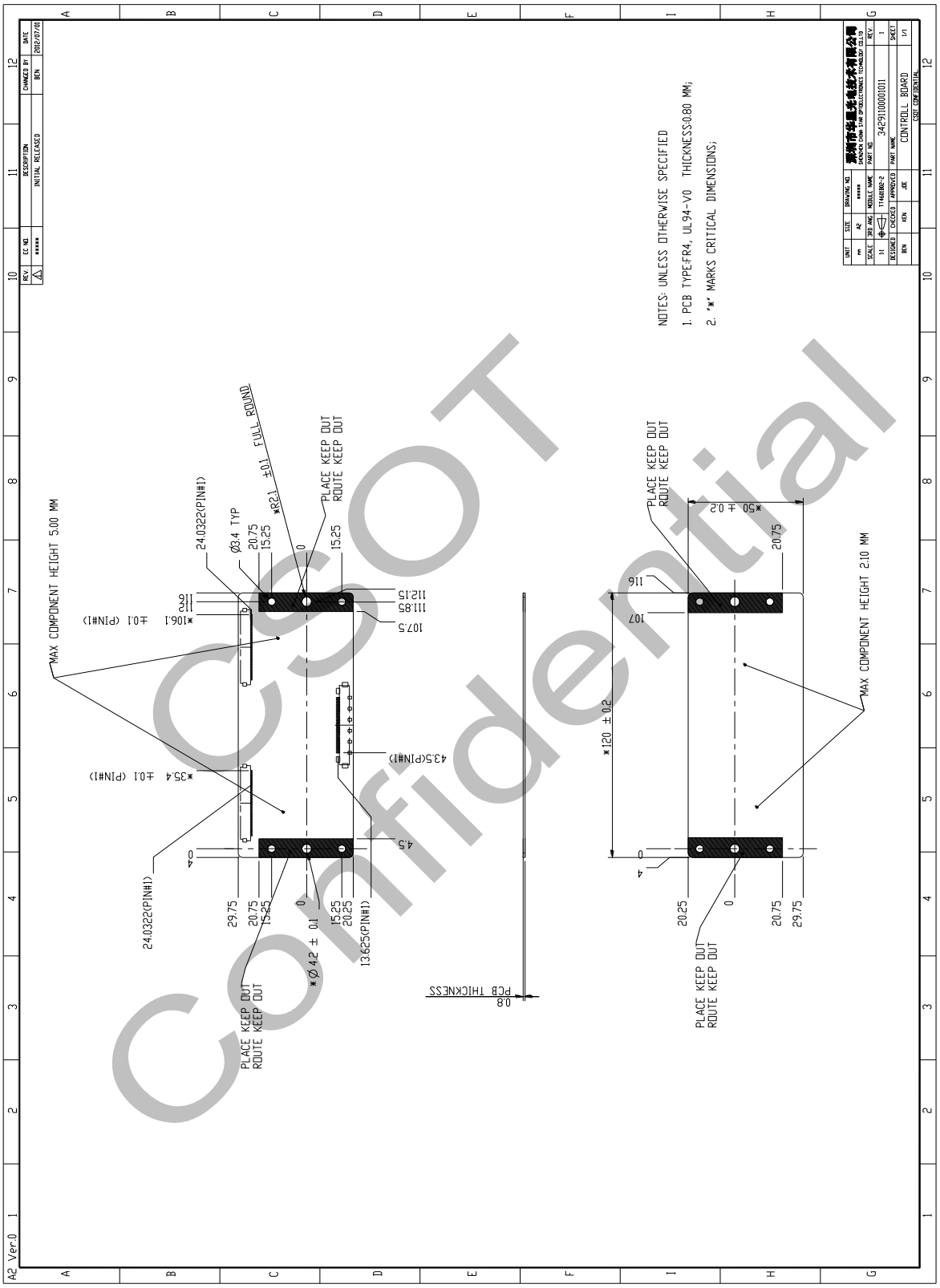
7. Mechanical Characteristics

7.1 Mechanical Specification

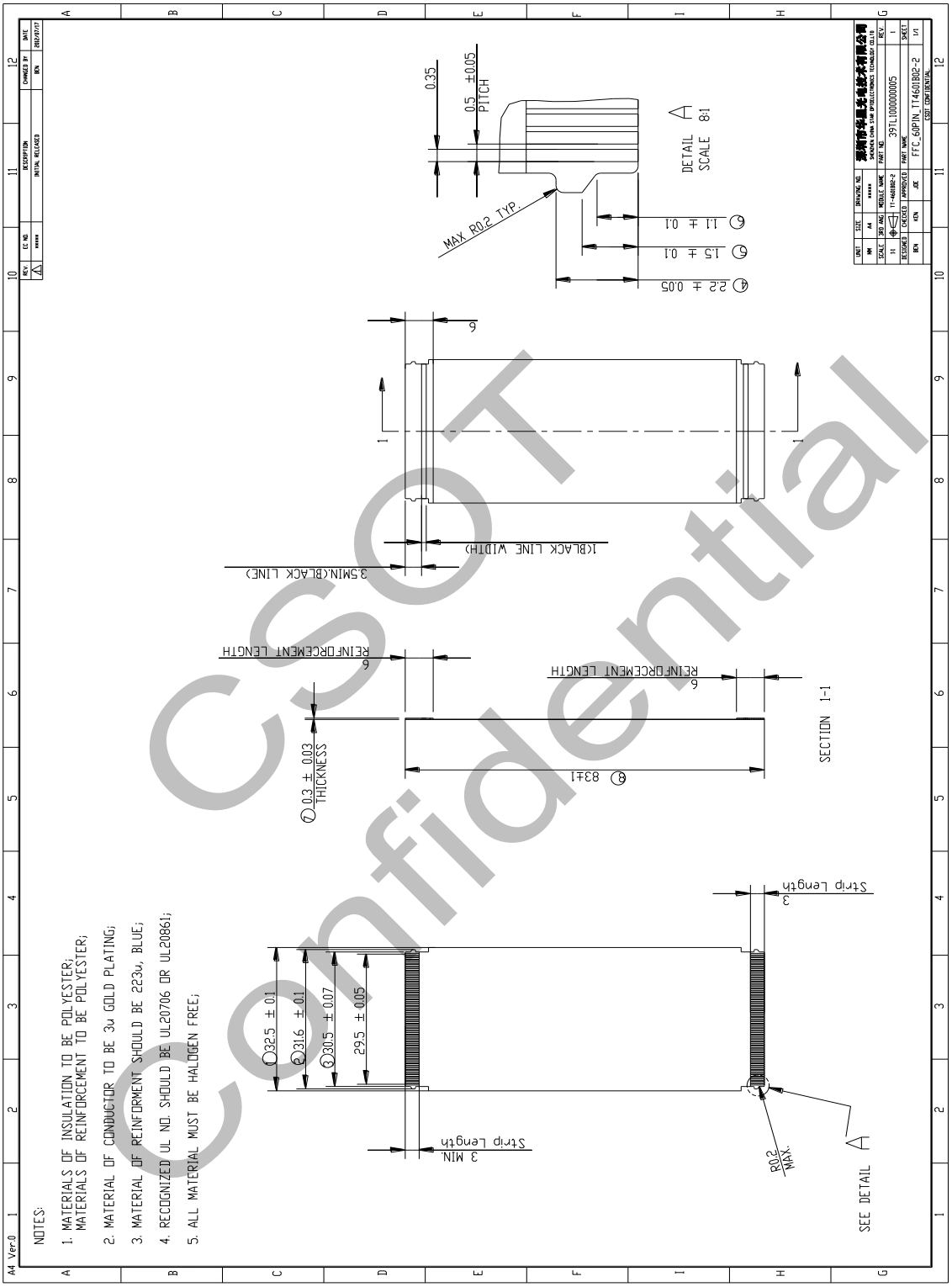
7.1.1 Open Cell Mechanical Specification



7.1.2 Control Board Mechanical Specification



7.1.3 FFC Mechanical Specification

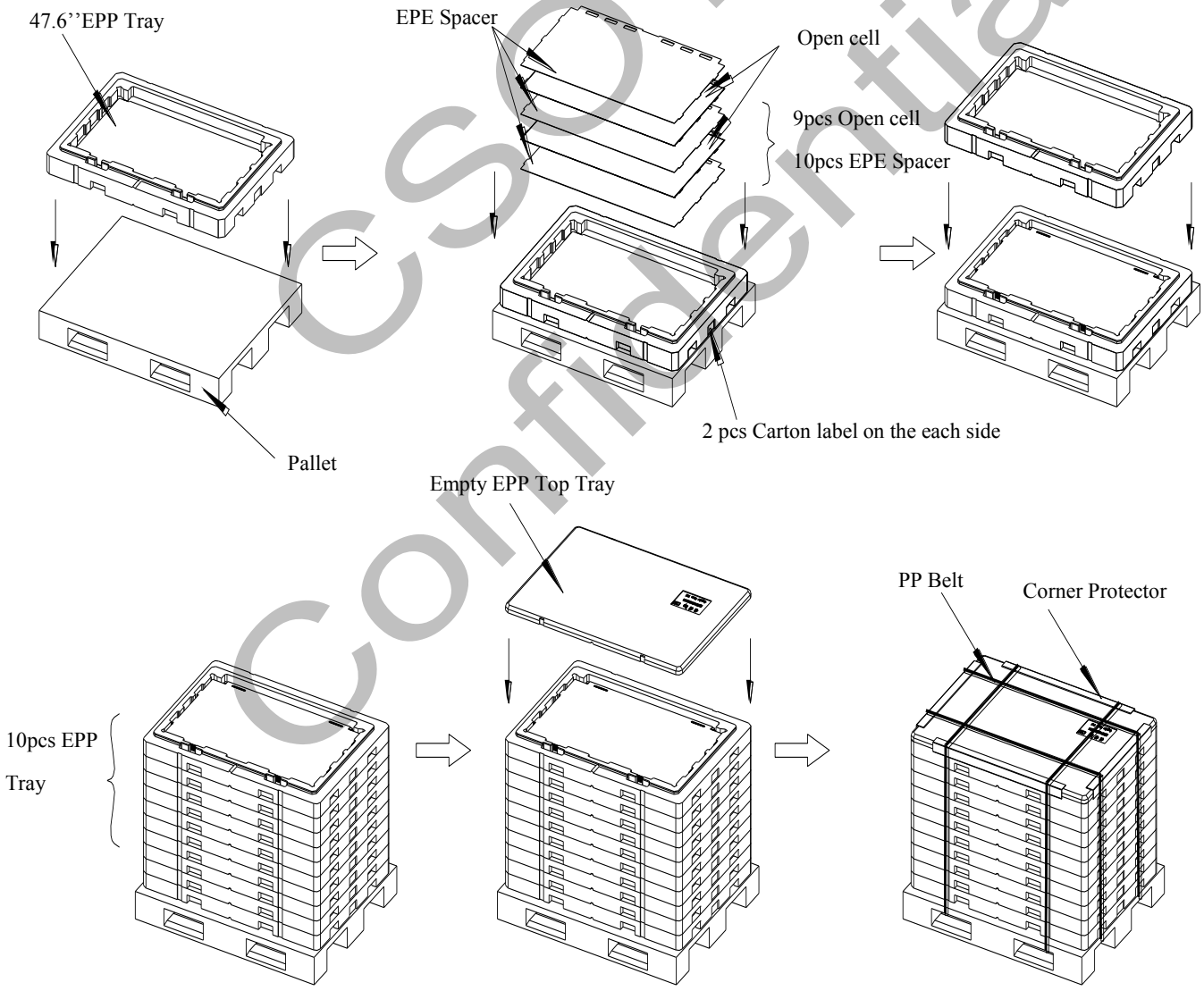


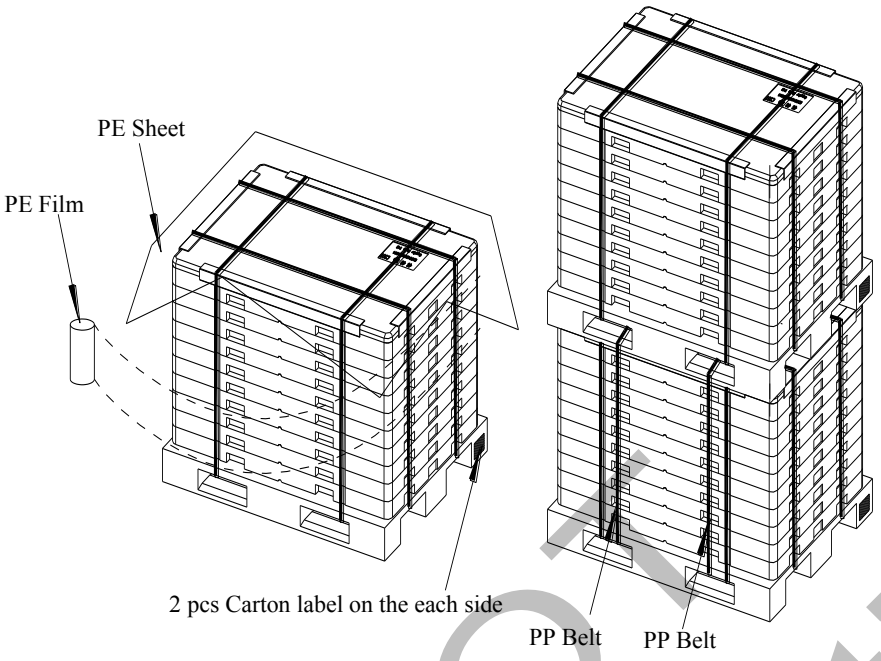
7.2 Packing

7.2.1 Open Cell Packing Specifications and Method

Item	Specification		
	Quantity	Dimension (mm)	Weight (kg)
Packing Box	9 pcs/box	1235(L) x 883 (W) x95 (H)	Net Weight: 18 (Max.) Gross Weight: 22(Max.)
Pallet	1	1250.00 (L) x 1000.00 (W) x 160.00 (H)	Net Weight:22
Stack Layer	10		
Boxes per Pallet	10boxes/pallet		
Pallet after Packing	90pcs/pallet	1250.0 (L) x 1000.0 (W) x 995.0 (H)	Gross Weight:244kg/pallet

Open Cell Packing Method

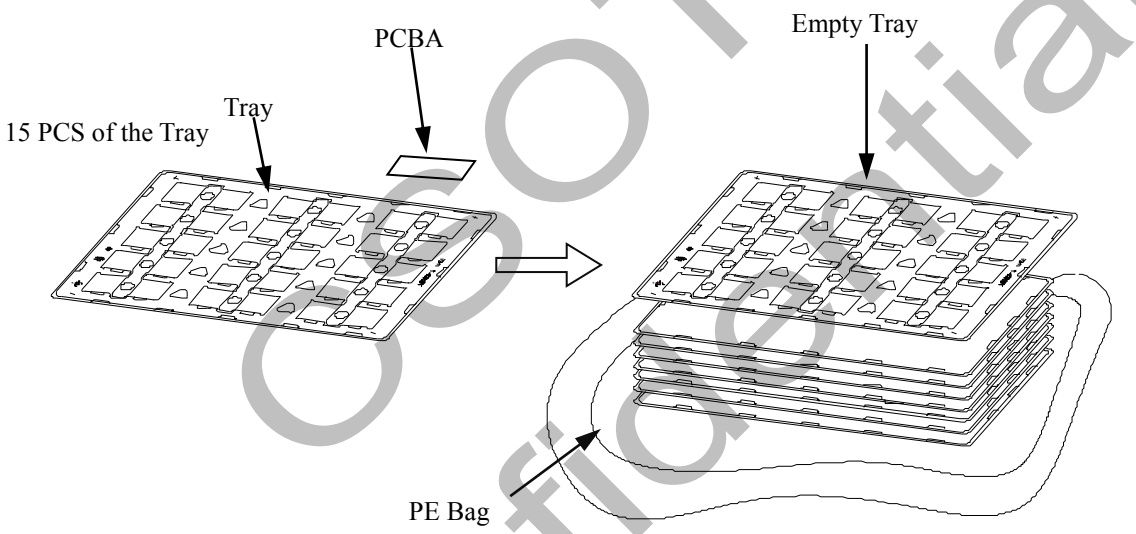


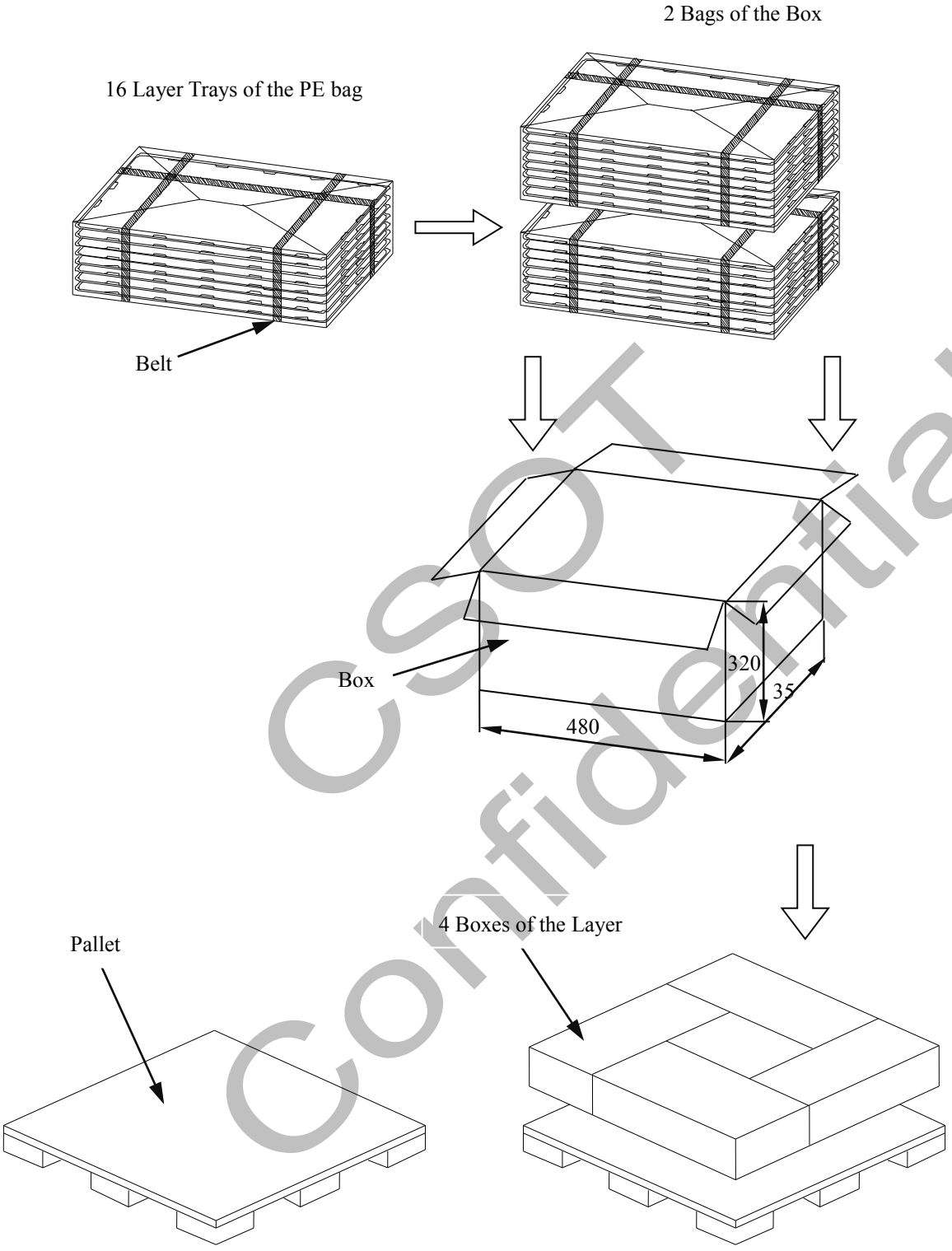


7.2.2 Control Board Packing Specifications and Method

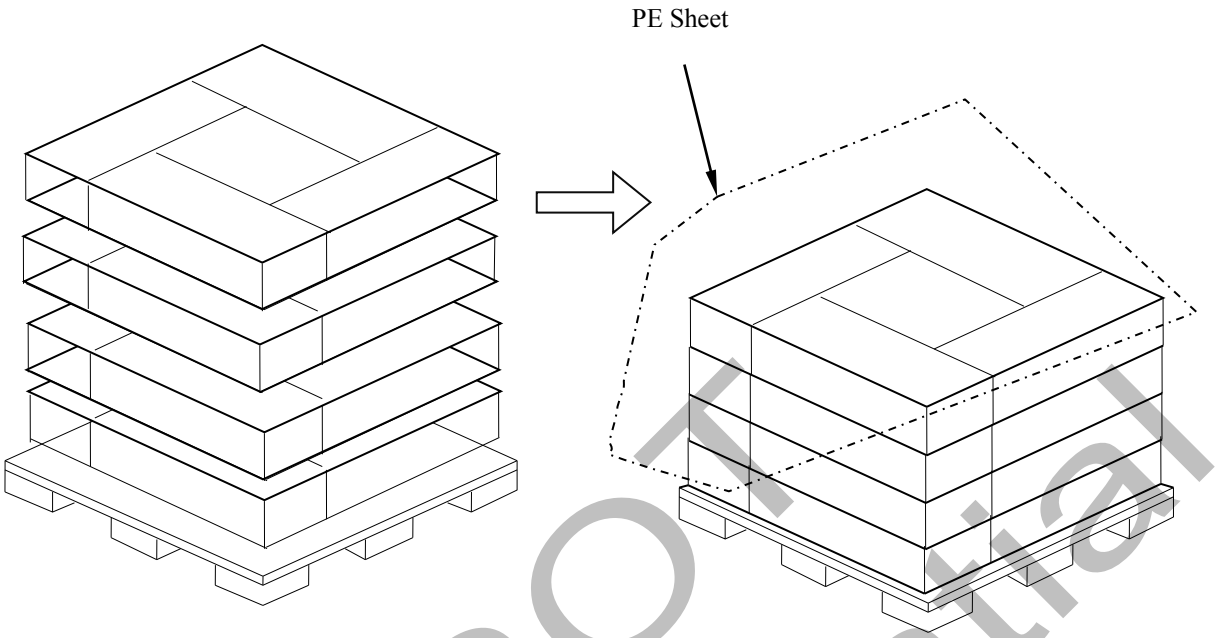
Item	Specification		
	Quantity	Dimension (mm)	Weight (kg)
Packing Box	390 pcs/box	570 (L) x 410 (W) x 320 (H)	Net Weight: 6.56 (Max.) Gross Weight: 13.48(Max.)
Pallet	1	1100 (L) x 1100 (W) x 120 (H)	Net Weight:16KG
Stack Layer	28(Include the one empty Tray)		
Boxes per Pallet	16boxes/pallet		
Pallet after Packing	6240pcs/pallet	1100 (L) x 11000 (W) x 1400 (H)	Gross Weight: 231.7kg/pallet

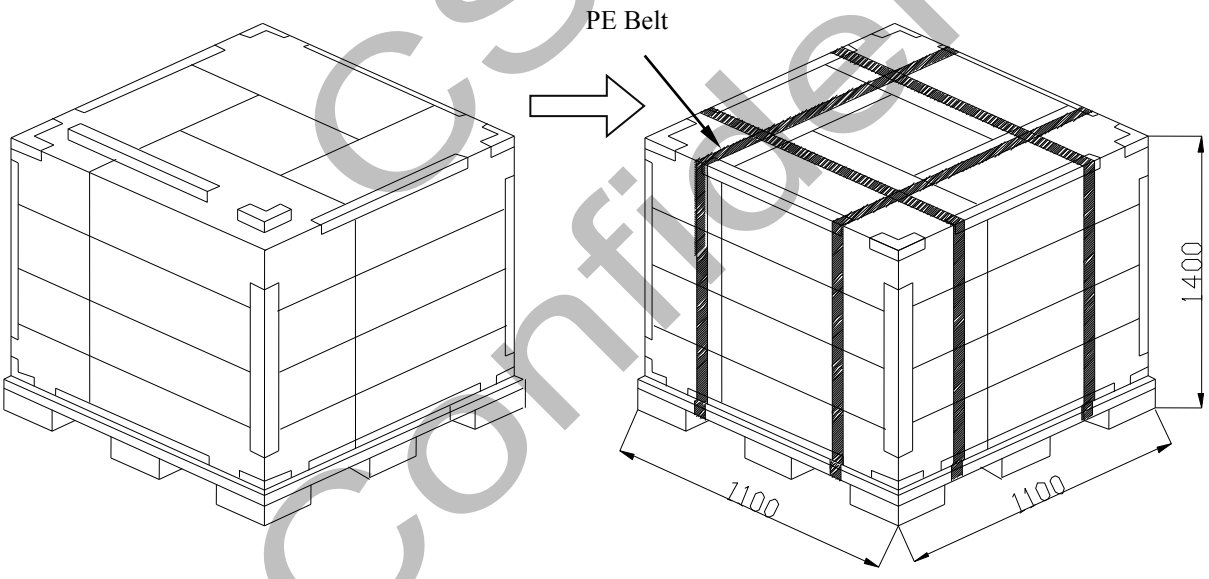
Control Board Packing Method





16 Boxes of the Pallet

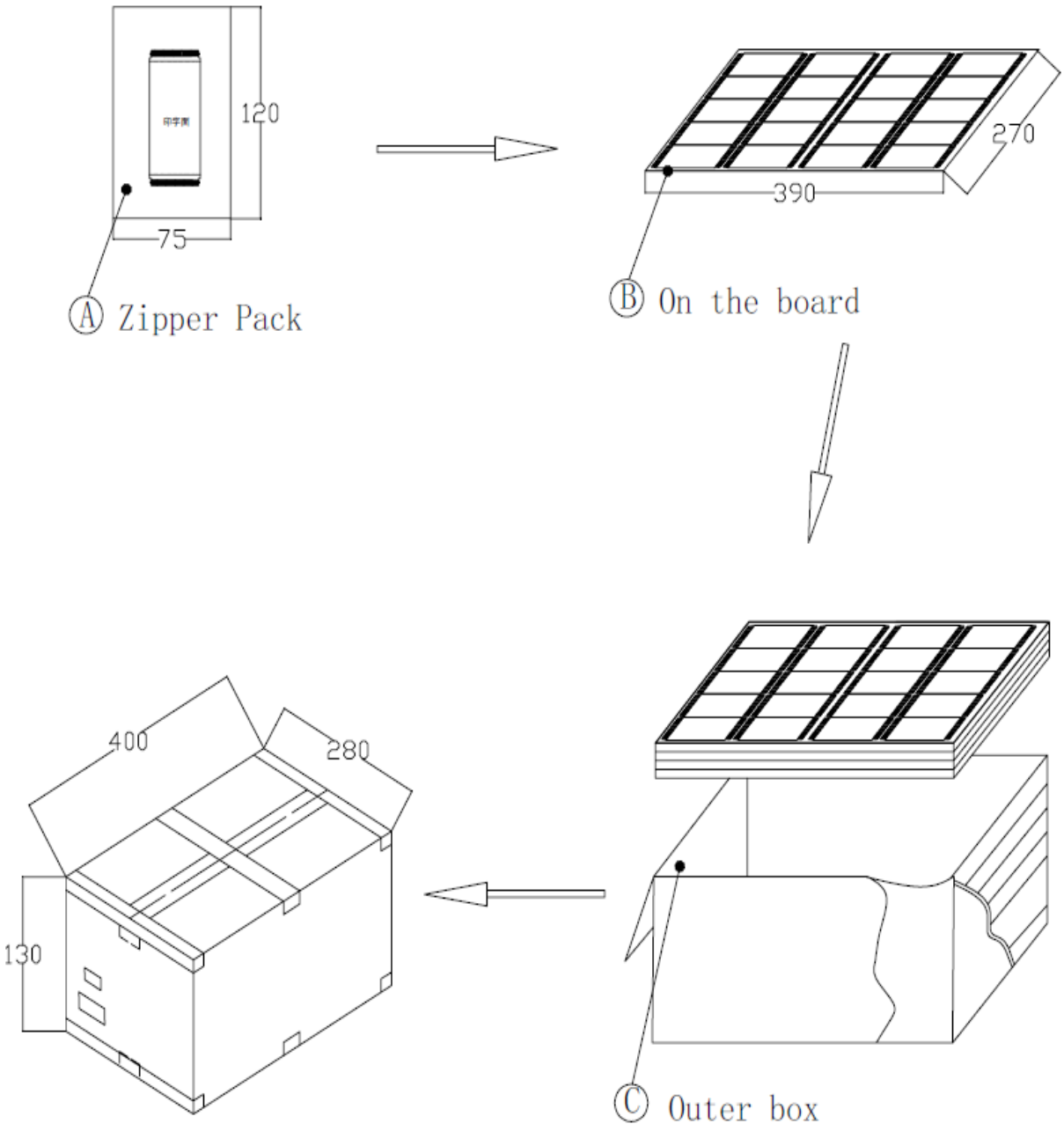




7.2.3 FFC Packing Specifications and Method

Item	Specification		
	Quantity	Dimension (mm)	Weight (kg)
Zipper pack	100 pcs/pack	120(L) x75(W)	
Box after packing	8000 pcs/box	400 (L) x 280 (W) x 130 (H)	Net Weight:9.6KG

FFC Packing Method



8. Definition of Labels

8.1 Open Cell Label

8.1.1 Open Cell Label

XXXXXXXXXXXXXXXXXXXX XXXX ST4761B01-3 Ver. X.X

- Model Version Code
- Model Name
- Week Code
- Serial Number

Serial Number: XXXXXXXXXXXX XXXXXXXX

- CSOT Internal Use
- Panel ID

Week Code: XX XX

- Week
- Year

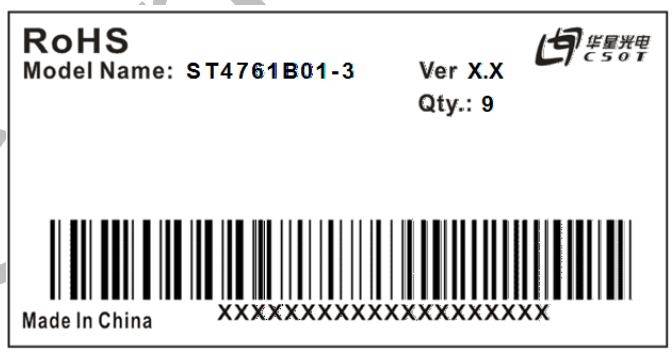
Year: 2010 =10, 2011 = 11 …2020= 20, 2021= 21…

Week: 01, 02, 03 …

Model Name: ST4761B01-3

Ver.X.X: Version, for example: 0.1, 0.2, … , 1.1, 1.2, …, 2.1, 2.2, …

8.1.2 Open Cell Carton Label



Serial Number: XXXXXXXXXXXXXXXXXXXX

- CSOT Internal Use
- Year, Month, Date
- Model Version Code
- CSOT Internal Use

8.1.3 Open Cell Pallet Label

Model Name: ST4761B01-3

Serial Number: XXXXXXXXXXXXX

- CSOT Internal Use
- Year, Month
- Model Version Code
- CSOT Internal Use

8.2 Control Board Label

8.2.1 Control Board Label

Part ID: 34291100006031

34291100006031 TDK B98 0L0 0200 0

- Prepare Number
- Serial Number
- CSOT Internal Use
- Manufactured Date
- CSOT Internal Use
- Part ID

Manufactured Date: B 9 8

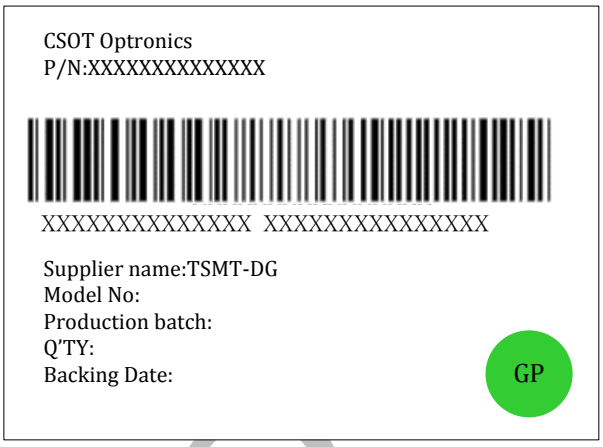
- Day
- Month
- Year

Year: 2012=B, 2013=C…

Month: 1, 2, 3 …A, B, C

Day: 1, 2, 3…A, B, C…

8.2.2 Control Board Carton Label



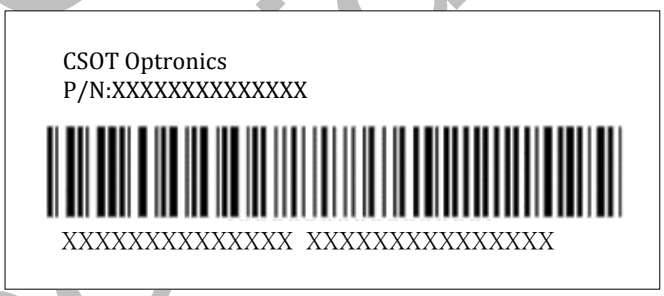
Part ID: 34291100006031

34291100005011XXXXXXXXXXXXXX

CSOT Internal Use

Part ID

8.2.3 Control Board Pallet Label



XXXXXXXXXXXXXXXXXXXXXXXXXXXXX

CSOT Internal Use

PCBA Q'ty

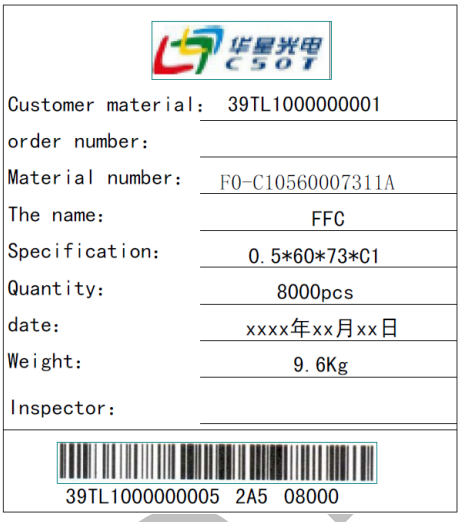
CSOT Internal Use

PCBA Manufactured Date

Part ID

CSOT Internal Use

8.3 FFC Carton Label



Serial Number: 39TL1000000005 2A5 08000

- 08000 → Quantity
- 2A5 → Date
- 39TL1000000005 → Product ID

9. Precautions

9.1 Assembly and Handling Precautions

(1) Do not apply rough force such as bending or twisting to the open cell during assembly.

(2) It is recommended to assemble or install a open cell into the user's system in clean working areas. The dust and oil may cause electrical shorter damage the polarizer.

(3) Do not apply pressure or impulse to the open cell to prevent the damage to the open cell.

(4) Always follow the correct power-on sequence. This can prevent the damage and latch-up to the LSI chips.

(5) Do not plug in or pull out the interface connector while the open cell is in operation.

(6) Use soft dry cloth without chemicals for cleaning because the surface of polarizer's very soft and easily be scratched.

(7) Moisture can easily penetrate into the open cell and may cause the damage during operation.

(8) High temperature or humidity may deteriorate the performance of the open cell. Please store open cell in the specified storage conditions.

(9) When ambient temperature is lower than 10ºC, the display quality might be deteriorated. For example, the response time will become slow.

9.2 Safety Precautions

(1) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(2) After the open cell end of life, it is not harmful in case of normal operation and storage.